07041 Abstracts Collection
Power-aware Computing Systems
— Dagstuhl Seminar —

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Abstract. From January 21, 2007 to January 26, 2007, the Dagstuhl Seminar 07041 "Power-aware Computing Systems" was held in the International Conference and Research Center (IBFI), Schloss Dagstuhl. During the seminar, several participants presented their current research, and discussed ongoing work and open problems. This report compiles abstracts of the seminar presentations as well as the seminar results and ideas, providing hyperlinks to full papers wherever possible.

Keywords. Power consumption, energy reduction, compilers, microarchitectures, simulations, experimental frameworks

07041 Summary – Power-aware Computing Systems

The program of the Dagstuhl seminar 07041 on Power-aware Computing Systems featured presentations of about 25 participating researchers from academia and industry. They were chosen to represent major areas in targeting the energy consumption of a computing system-Applications, Compilers, Virtual-execution Environments, Operating Systems, and Hardware. In order to continue the work of the predecessor Dagstuhl seminar held in 2005, the results of that seminar [1] were discussed, with the aim of developing a vision of challenges, problems, and research activities in some of the key areas identified in 2005. The first part of the seminar was dedicated to lively discussions that led to the identification of three areas that were considered being most interesting. As a result, three groups were formed to further identify challenges and opportunities. The results of these groups are presented in this report. In addition, abstracts of the presentations as well as work-in-progress papers are published in these proceedings.

Keywords: Power-aware Computing Systems, Low-power Design, Parallelism and Power Consumption

Joint work of: Benini, Luca; Chang, Naehyuk; Kremer, Ulrich; Probst, Christian W.

Extended Abstract: http://drops.dagstuhl.de/opus/volltexte/2007/1123

07041 Working Group – Towards Interfaces for Integrated Performance and Power Analysis and Simulation

In the design and optimization of power-aware computing systems, it is often desired to estimate power consumption at various levels of abstraction, e.g., at the transistor, gate, RTL, behavioral or transaction levels. Tools for power estimation at these different levels of abstraction require specialized expertise, e.g., understanding of device physics for circuit-level power estimation, and as such are necessarily developed by different research communities.

In the optimization of complete platforms however, it is desired to be able to obtain aggregate power and performance estimates for the different components of a system, and this requires the ability to model the system at a mixture of levels of abstraction.

One approach to enabling such cross-abstraction modeling, is to define a mechanism for interchange of data between tools at different layers of abstraction, for both static analysis and simulation-based studies. This document presents preliminary discussions on the requirements of such an interface.

Keywords: Power Estimation Tools, Simulation, Tool Interfaces

Joint work of: Bleakley, Chris; Clerckx, Tom; Devos, Harald; Grumer, Matthias; Janek, Alex; Kremer, Alex; Kremer, Ulrch; Probst, Christian W.; Stanley-Marbell, Phillip; Steger, Christian; Venkatachalam, Vasanth; Wendt, Manuel

Extended Abstract: http://drops.dagstuhl.de/opus/volltexte/2007/1107

Thermal Characterization and Thermal Management in Processor-Based Systems

José Luis Ayala (Technical University of Madrid, E)

As technology scales down and the low-power techniques are implemented, the temperature characterization and the power-aware design methodologies emerge. Several thermal characterization techniques based on electrical measures, on-chip sensors or mathematical models can be devised. This talk will provide an overview of how these novel techniques can be used to perform a thermal map in processor-based systems.

Moreover, the impact on temperature of several design factors (placement, topology, etc) and software variables (source-code transformations) is analyzed and some conclusions are drawn. These conclusions can lead the future temperature-aware compilation.

Joint work of: Ayala, José Luis; Apavatjrut; Anya; Atienza, David; López-Vallejo, Marisa; López-Barrio, Marisa

Extended Abstract: http://drops.dagstuhl.de/opus/volltexte/2007/1110

Electrocardiogram in Wireless Sensor Nodes

Mladen Berekovic (Stichting IMEC Nederland - Eindhoven, NL)

The talk gives an overview of IMEC's program for wireless autonomous transducer systems (WATS) with a focus on the concepts for ultra-low-power autonomous signal processing. Investigations have shown that most of the power in classical sensor nodes is spent for wireless transmission of the sample data. If, for example, the data for a heart beat detection is processed locally in the sensor node, then the sample transmission rate can be reduced by an order of magnitude leaving more energy for local signal processing. The talk also gives some examples of how these goals can be reached using signal processing techniques above 500 MOPs/mW.

Joint work of: Yseboodt, Lennart; De Nil, Michael; Berekovic, Mladen

Keywords: Low-power, WATS, wireless sensor nodes

Extended Abstract: http://drops.dagstuhl.de/opus/volltexte/2007/1111

Full Paper:
www.imec-nl.nl

Instantaneous Current Modeling at the Instruction Level

Chris Bleakley (University College - Dublin, IRL)

Estimation of processor current consumption is important for the design of low power systems. This paper proposes a novel method for estimating the dynamic current consumption of a processor. The method models dynamic current as the output of a linear system excited by a signal comprised of the total current due to each instruction. System identification is performed by cross-correlation of a pseudo-random stimulus with the measured current. The method was applied to the Texas Instruments TMS320VC5510 DSP processor and was found to provide an average correlation of 93% between the estimated and measured dynamic current across a range of benchmarks.

Keywords: Power estimation, DSP

Joint work of: Bleakley, Chris; Casas-Sanchez, Miguel; Rizo-Morente, Jose

See also: J. Rizo-Morente, M. Casas-Sanchez and C.J. Bleakley (2006) "Dynamic Current Modelling at the Instruction Level", Proc. IEEE/ACM Int. Symp. on Low Power Electronics and Design (ISLPED), pp. 95-100, Tegernsee, Germany, October 2006.

Fuel Cell and Battery Hybrid System Platform for Human-Portable Embedded Applications

Naehyuck Chang (Seoul Nat. University, ROK)

Due to increasing energy consumption of microelectronics, many techniques have been developed for reducing total system energy consumption, with reasonable tradeoffs in performance or quality of service (QoS). Despite these efforts, many portable applications now require next generation power sources that have a higher energy density for longer operational time, power sources such as a fuel cell.

A Proton Exchange Membrane Fuel Cell (PEMFC) operates in room temperature, and its power density is 4 to 6X larger than that of Lithium ion batteries. However, due to its limited power capacity and slow response to immediate power demands, a more practical approach would be to use a fuel cell and battery hybrid, thereby combining the high energy density of the fuel cell with the high power density of a battery.

In this talk, we introduce a fuel cell and battery hybrid system for portable applications. It includes a fuel processor subsystem, a PEMFC stack and its controller subsystem, and a charge management subsystem. Our recent work showed that power management policies of embedded systems powered by such a hybrid should be different from those of conventional systems. Thus, our aims are to characterize the hybrid system performance and characteristics, to develop new power management policies, and finally to confirm the feasibility and performance of the new power management schemes that we have developed.

The proposed platform can accommodate 20W average power and up to 100W peak power, powered by sodium borohydride solution as a fuel. It is equipped with dual Li-ion batteries for the enhancement of the battery charging and discharging efficiency. Its features have been fully demonstrated at ACM SIGDA University Booth of the 2006 Design Automation Conference.

Keywords: Fuel cell, power management, lowpower, portable

Full Paper:
http://cselab.snu.ac.kr/member/naehyuck

See also: Naehyuck Chang received BS, MS and PhD degrees from the Department of Control and Instrumentation, Seoul National University, in 1989, 1992 and 1996 respectively. He has been with the School of Computer Science and Engineering since 1997 and now is an Associate Professor. He has been with Arizona State University as well, since 2005. He has also been serving as

a Technical Advisor of Sindoricoh, Co. Ltd. since 2001. His research interest is embedded systems and low-power systems design and implementation, and he has published over 50 technical papers in these areas.

Integrated CPU and L2 Cache Frequency/Voltage Scaling using Supervised Learning

Bruce R. Childers (University of Pittsburgh, USA)

Multiple clock domain (MCD) processors can provide independent power management in different chip units with dynamic frequency/voltage scaling (DFVS). A significant power and energy improvement is possible with independent and fine-grain control of DFVS for each domain. A typical DFVS control policy for an MCD processor manages each domain in isolation due to the complexity of deriving a global policy that considers all domains. However, there is a potential for domain interactions, which can affect the achieved power and energy savings with these policies. In this talk, I will describe an approach based on supervised machine learning that automatically derives a global control policy for an MCD processor that considers domain interactions.

From experimental results, we have found that a derived policy saves up to 34% (10% in the average case) more energy than a policy that independently manages the domains.

Distributed Video Coding: The Inverse Coding Paradigm

Tom Clerckx (Vrije Universiteit Brussel, B)

In the past, video coding architectures have primarily been typecasted as downlink systems. That is, they consist of complex encoding mechanisms running on powerful machines, while the decoder is executed on devices which have only a fraction of the computational power of the encoder. In this design the encoders are positioned at fixed locations, while the decoders maintain means of mobility.

Today, with the scaling of technologies and the usage of high-computational low-power mobile devices, the desire has grown to also code video on these type of microcomputers. This means however, that the downlink-model is no longer valid and that new systems have to be designed that can cope with the challenges of low-complex encoding/decoding mechanisms, robustness against transmission-errors, and high compression efficiency.

Distributed video coding (DVC) is a video coding system, which has the potential to simultaneously meet these requirements. DVC is based on the theoretical paper of Slepian and Wolf on noiseless coding of correlated information sources, which was later extended for lossy coding by Wyner and Ziv. In typical DVC systems, the encoder uses simple forward error-correcting mechanisms to

encode the source in a distributed fashion. It is then the decoder's task to exploit inter-source correlations by means of motion-compensated interpolation.

The goal of this talk is to give a global overview of the principles of distributed video coding, as well as to give some more detailed information about my research in this area, which involves applying motion-estimation in a DVC system. An informal discussion afterwards, may lead us to potential new research tracks.

Keywords: Distributed Source Coding, Slepian Wolf, Wyner Ziv, Low complexity

Energy Scalability and the RESUME Scalable Video Codec

Harald Devos (Gent University, B)

In the context of the RESUME-project (http://elis.ugent.be/resume) a scalable wavelet-based video decoder was built to demonstrate the benefits and flexibility of reconfigurable hardware for scalable applications.

By "scalable" we mean that it allows one to easily change the quality of service (QoS) (i.e., the frame rate, resolution, color depth) of the decoded video without having to change the video stream used by the decoder (except for skipping unnecessary blocks of data without decoding) or having to decode the whole video stream if only part of it is required.

With the emergence of high-performance field programmable gate arrays, the required performance for real-time decoding and the flexibility for allowing reconfiguration are offered.

Energy measurements show how the energy consumption of the decoder can be scaled by varying the decoding quality.

Keywords: Scalable video, wavelet, FPGA, energy

Joint work of: Devos, Harald; Eeckhaut, Hendrik; Christiaens, Mark

Energy Scalability and the RESUME Scalable Video Codec

Harald Devos (Gent University, B)

In the context of the RESUME-project a scalable wavelet-based video decoder was built to demonstrate the benefits of reconfigurable hardware for scalable applications. *Scalable* video means that the quality of service (QoS) (i.e., the frame rate, resolution, color depth) of the decoded video can easily be changed by only decoding those parts of the video stream that contribute to the desired QoS.

With the emergence of high-performance FPGAs (Field Programmable Gate Array), both the required performance for real-time decoding and flexibility, by allowing reconfiguration, are offered.

Since the amount of calculations scales with the QoS, energy dissipation is expected to scale similarly. To investigate the relation between QoS and energy dissipation we actually measured the energy dissipation of a scalable video decoder implementation on a FPGA. The measurements show how dissipation effectively scales with the QoS, but also depends on the decoded data and the used design method. This is illustrated by comparing two different implementations of the inverse discrete wavelet transform (IDWT).

Keywords: Wavelet-based Scalable Video, Energy Measurement, Hardware Generation, FPGA

Joint work of: Devos, Harald; Eeckhaut, Hendrik; Christiaens, Mark; Stroobandt, Dirk

Full Paper: http://drops.dagstuhl.de/opus/volltexte/2007/1112

Dynamic Adaptive Power Management For–And By–A Java Virtual Machine

Andreas Gal (Univ. California - Irvine, USA)

Traditionally, adaptive power management has been performed at the operating system (OS) level. We present a dynamic adaptive power management plugin for the Java Virtual Machine (JVM) that improves the precision of power management decisions by utilizing fine-grained high-level program state information available to the virtual machine, but often invisible to the OS. In contrast to power management components situated at the OS level, our virtual machine plugin injects runtime profiling probes and power management triggers at the Java bytecode-level and is thereby independent of target architecture, JVM implementation, and host operating system.

Keywords: Java Virtual Machine, Dynamic Voltage Scaling, Power Management, Profile-Guided Optimization

Joint work of: Gal, Andreas; Rauch, Michael; Franz, Michael

Software Power Peak Reduction on Different Compiler Levels for Mobile Devices

Matthias Grumer (TU Graz, A)

The complexity of embedded systems is continuously growing due to the increasing requirements for performance. In portable systems such as smart cards, performance is not the only important attribute, but so is the power and energy consumed by a given application.

Sources of energy used in smart card systems such as batteries and electromagnetic fields are nonideal, because their effectiveness depends heavily on the energy consumed over time. Optimization strategies proposed so far are implemented statically. Often a manual measurement of the current profile followed by manual optimizations is carried out. This procedure is very time consuming. We present a method for flattening the power profile of an application based on a compiler optimization. Optimizations on different compiler levels will be presented.

Compiler-based Software Power Peak Elimination on Smart Card Systems

Matthias Grumer (TU Graz, A)

RF-powered smart cards are widely used in different application areas. For smart cards, performance is not the only important attribute, but so is the power consumed by a given application. The power consumed depends heavily on the software executed on the system. The power profile, and especially the power peaks, of an executed application influence the system stability and security. Flattening the power profile can thus increase the stability and security of a system.

In this paper we present a compiler optimization based system that allows a reduction of the power peaks. The optimizations are performed at different levels of the compiler. In the back end of the compiler, we present new instruction scheduling algorithms. At the intermediate language level, we propose the use of iterative compiling for reducing critical peaks.

Keywords: Software power optimization, compiler optimization, peak reduction

Joint work of: Grumer, Matthias; Wendt, Manuel; Steger, Christian; Weiss, Reinhold; Neffe, Ulrich; Muehlberger, Andreas

Full Paper: http://drops.dagstuhl.de/opus/volltexte/2007/1103

Power Management Strategies and Energy Storage Structures for Battery-driven Higher Class UHF RFID Tags

Alex Janek (CISC - Klagenfurt, A)

The next generation of RFID tags (higher class tags - HCT) especially in the UHF frequency range provides extended functionality, such as high operating range and sensing and monitoring capabilities including data acquisition units, real time clocks and active transmitters. This causes a high energy consumption

of the tag and requires an on-board energy store (battery). The charge state of this energy reservoir defines the lifetime of the HCT and thus the reliability of the whole RFID system.

The PowerTag project deals with proposing special power management algorithms and energy store structures in combination with the use of energy harvesting devices to support the on-board battery. This allows for extending the lifetime of the HCT, providing high level computational and peripheral functionality.

Full Paper: http://drops.dagstuhl.de/opus/volltexte/2007/1104

Lifetime Extension of Higher Class UHF RFID Tags Using Special Power Management Techniques and Energy Harvesting Devices

Alex Janek (CISC - Klagenfurt, A)

Enhanced RFID tag technology especially in the UHF frequency range provides extended functionality like high operating range and sensing and monitoring capabilities. Such functionality requiring extended system structures including data acquisition units, real time clocks and active transmitters causes a high energy consumption of the tag and requires an on board energy store (battery). Since a key parameter of the reliability of an RFID system is the lifetime, the energy budget of the higher class tag has to be as balanced as possible. This can be achieved by using energy harvesting devices as an additional power supply. The PowerTag project and this paper propose special power management mechanisms in combination with special energy storage structures interfacing with energy harvesting devices and dealing with their special requirements. First, various power management techniques are simulated and their performance is evaluated. In a second step, different variants of energy storage structures are compared by using accurate simulation models of the various parts of the system. The results are compared to manufacturer-given and guaranteed system performance parameters of a state-of-the-art higher class UHF RFID system. The presented approach combines two simulations for the design and the evaluation of different tag architectures and power saving techniques. Simulation results, applying the techniques this paper discusses, are showing an improvement of over 44% of the achievable lifetime, compared to a state-of-the-art higher class system.

Keywords: Higher Class UHF RFID, Energy harvesting, Energy storage architectures, Lifetime extension

Joint work of: Janek, Alex; Steger, Christian; Preishuber-Pfluegl, Josef; Pistauer, Markus

Efficient Program Power Behavior Characterization

Ulrich Kremer (Rutgers Univ. - Piscataway, USA)

Fine-grained program power behavior is useful for evaluating power optimizations and observing power optimization opportunities. Detailed power simulation is time consuming and often inaccurate. Physical power measurement is faster and objective. However, coarse-grained measurement sacrifices important detail, while fine-grained measurement generates enormous amounts of data in which locating important features is difficult.

We present a program power behavior characterization infrastructure that identifies program phases, selects a representative interval of execution for each phase, and instruments the program to enable precise power measurements of these intervals to get their time-dependent power behavior.

Keywords: Time-dependent power behavior; power measurement infrastructure

Joint work of: Hu, Chunling; Daniel A. Jimenez; Kremer, Ulrich

Post-Silicon Thermal-Aware Clock Distribution Network Design

Massimo Poncino (Politecnico di Torino, I)

The thermal gradients arising in high-performance circuits may significantly affect their timing behavior, in particular by increasing the skew of the clock net or altering hold/setup constraints, possibly causing the circuit to operate incorrectly. The knowledge of the spatial distribution of temperature can be used to properly design a clock network that is able to compensate for such thermal non-uniformities. However, re-design of the clock network is effective only if temperature distribution does not change over time.

In this talk, we address the problem of post-silicon tuning of the clock tree in such a way that it can compensate for variations of temperature over time. This is achieved by selectively replacing buffers that are inserted during the clock network generation with tunable delay elements. Temperature-induced delay variations are then compensated by applying the proper tuning to the tunable buffers, which is computed off-line and stored in a tuning table inserted in the design.

We present an algorithm to minimize the number of inserted tunable buffers, as well as their tunable range, which directly relates to complexity. Results show that the clock skew can be kept within original bounds with minimal area and power penalty.

Keywords: Thermal-aware design, clock tree synthesis

See also: Dynamic thermal clock skew compensation using tunable delay buffers, ISLPED'06

Complexity of Scheduling in Synthesizing Hardware from Concurrent Action Oriented Specifications

Gaurav Singh (Virginia Polytechnic Institute, USA)

CAOS (Concurrent Action Oriented Specifications) is a new model of computation for specifying hardware designs as exemplified by the Bluespec System Verilog. In addition to the easy resolution of concurrency issues, CAOS provides a higher abstraction level than behavioral RTL, and provides the opportunity for automatic hardware synthesis through tools such as the Bluespec Compiler (BSC). In the recent past, BSC has been shown to produce area and performance efficient hardware designs comparable to hand-written HDL. However, due to the increasing demand of powerefficient designs, it is crucial to make such synthesis power-aware. This presentation talks about low-power hardware synthesis from CAOS.

Keywords: Low-power, Synthesis

Joint work of: Singh, Gaurav, Ravi, S. S.; Ahuja, Sumit; Shukla, Sandeep

Full Paper: http://drops.dagstuhl.de/opus/volltexte/2007/1105

Power Awareness vs. Transparency

Jens Sparsø (Technical University of Denmark, DK)

An issue I would like to discuss at the workshop is to what extent "power awareness" implies "transparency" in the sense that a programmer can understand and influence the power consumption of his/her program, given todayŠs architectures and programming models. Obvious issues to consider are the (cache) memory hierarchy and communication in (heterogeneous) multi-processor systems-on-chip.

The SFLR Toolsuite — Hardware and Software Research Platforms for Energy-Constrained and Failure-Prone Systems

Phillip Stanley-Marbell (TU of Eindhoven, NL)

Research in any field requires tools that enable the modeling of system characteristics of interest. Such tools, whether analytic, simulative or hardware, must enable the accurate representation of all the aspects of a system that may influence the system's perceived utility.

Software tools (notably, simulators) provide low cost of entry, flexibility, and low turn-around time in investigations, but often abstract away some hardware details, with loss in accuracy and realism. Hardware implementations provide the

ultimate proof of concept, but are usually expensive, inflexible, and not always designed to expose all possible system parameters to researchers; they are also often not actively evolved over time as research platforms in their own right.

This talk describes a suite of tools, comprising a full-system (embedded microarchitecture, networking, power, battery and analog signal) simulator, a miniature energy-scavenging hardware sensor platform, and a handheld interface device (work in progress). The suite is intended to provide a complementary and comprehensive platform for research in micro-architectures and system-architectures for embedded systems, with attention to energy-efficiency, reliability, and ecological impact.

Keywords: Hardware platforms, Simulation, Dynamic Voltage Scaling, Energy-Scavenging, Fault-Tolerance

Extended Abstract: http://drops.dagstuhl.de/opus/volltexte/2007/1106

Power Optimization of Ubiquitous Devices like Smart Cards and Future RFID Tags

Christian Steger (TU Graz, Austria)

The presentation gives a motivation of recent research projects in the area of power awareness at the Institute of Technical Informatics. Furthermore the aim is to lead over to the presentations of Matthias, Manuel and Alex.

Towards Class-Based Dynamic Voltage Scaling for Multimedia Applications

Richard Urunuela (Ecole des Mines de Nantes, F)

Video kiosks increasingly contain powerful PC-like embedded processors, allowing them to display video at a high level of quality. Such video display, however, entails significant energy consumption. This paper presents an approach to reducing energy consumption by adapting the CPU clock frequency. In contrast to previous approaches, we exploit the specific behavior of a video kiosk. Because a kiosk plays the same set of movies over and over, we choose a CPU frequency for a given frame based on the computational requirements of the frame that were observed on earlier iterations. We have implemented our approach in the legacy video player MPlayer. On a PC like those that can be found in kiosks, we observe increases in battery lifetime of up to 2 times as compared to running at the maximum CPU frequency on a set of high resolution divx movies.

Keywords: Dynamic voltage scaling, multimedia application, embedded systems

Full Paper: http://drops.dagstuhl.de/opus/volltexte/2007/1108
Full Paper:
http://www.emn.fr/x-info/rurunuel

Self-Calibrating Processor Speed: A New Feedback Loop for Dynamic Voltage Scaling Control

Vasanth Venkatachalam (Univ. California - Irvine, USA)

The benefit of dynamic voltage scaling depends on how compute-bound a workload is. The more time a processor stalls, the more the workload can be slowed down without incurring a proportional performance loss. However, determining a measure of "compute-boundedness" is nontrivial. This property has often been inferred from secondary effects, such as cache miss rates.

We propose a new mechanism for extrapolating compute-boundedness from minute variations of processor speed. By adjusting the processor speed by just a small amount, and extrapolating from the difference in execution cycles, we can precisely estimate a workload's execution time at any processor speed. Moreover, simulation results suggest that frequency steps can be far smaller than the hundreds of megahertz supported by typical laptops. In fact, by adjusting the processor speed by as little as tens of megahertz, we can gather enough data to predict execution times for frequency adjustments on the order of hundreds of megahertz.

This leads to a new lightweight approach to CPU clock scaling called the "self-calibrating feedback loop". Rather than relying on indirect information from hardware events our approach relies on direct observation of what happens when the processor is slowed down during program execution.

Keywords: Performance, estimation, power management, dynamic voltage scaling, clock frequency

Automist - A Tool for Automated Instruction Set Characterization of Embedded Processors

Manuel Wendt (TU Graz, A)

The steadily increasing performance of mobile devices also implies a rise in power consumption. To counteract this trend it is mandatory to accomplish software power optimizations based on accurate power consumption models characterized for the processor. This paper presents an environment for automated instruction set characterization based on physical power measurements. Based on a detailed instruction set description a testbench generator creates all needed test programs for a complete characterization. Afterwards those programs are executed by the processor and the energy consumption is measured. For an accurate energy measurement a high performance sampling technique has been established, which can be either clock or energy driven.

Keywords: Software energy estimation, automated processor characterization, testbench generator, current measurement, clock driven sampling, energy driven sampling.

Joint work of: Wendt, Manuel; Grumer, Matthias; Steger, Christian; Neffe, Ulrich

Full Paper: http://drops.dagstuhl.de/opus/volltexte/2007/1109

Temperature-aware Design Automation Techniuqes and Future Challenges

Yuan Xie (Pennsylvania State University, USA)

This talk will give an overview of thermal-aware design automation techniques developed at Pennsylvania State University, and discuss future challenges.

Keywords: Thermal