Dynamically Reconfigurable Architectures
Dagstuhl Seminar 10281
Proceedings Abstract

P. Athanas, J. Becker, J. Teich, I. Verbauwhede

Dynamic and partial reconfiguration of hardware architectures such as FPGAs and coarse grain processing arrays bring an additional level of flexibility in the design of electronic systems by exploiting the possibility of configuring functions on-demand during run-time. When compared to emerging software-programmable Multi-Processor System-on-a-Chip (MPSoC) solutions, they benefit a lot from lower cost, more dedication and fit to a certain problem class as well as power and area efficiency. This has led to many new ways of approaching existing research topics in the area of hardware design and optimization techniques. For example, the possibility of performing adaptation during run-time raises questions in the areas of dynamic control, real-time response, on-line power management and design complexity, since the reconfigurability increases the design space towards infinity.

This Dagstuhl Seminar on Reconfigurable Architectures has aimed at raising a few of the above topics. In the **methodological** area, on-line placement, pre-routing/on-line routing and dynamic compaction algorithms and techniques were presented. In the **architectural** realm, novel interconnection schemes as well as hypermorphic architectures for the future of reconfigurable computing systems in general were introduced and discussed. A major question here was whether programmable multi-core Systems-on-a-Chip (MPSoC) will win margins for typical application domains such as rapid prototyping and emulation and how to scale reconfigurable hardware further in the threat of diminishing returns due to more and more unreliable components of future nano-electronic devices. Also questioned were **tool maturity** and recent developments in the usage of reconfigurable computing for increase of **fault-tolerance**. Finally, for the first time, a special focus day was spent on the area of **embedded security** and the role of reconfigurable hardware in this emerging and important application area.

The workshop started on Sunday evening. After arrival, the attendees joined each other for dinner and discussions, before watching together the soccer world cup final.

The sessions on Monday lead by Jürgen Becker were dedicated to the topic: “Future Technologies: Online Adaptivity - A must for future applications and (nano) technologies”. After a brief opening session, he started the topic, by giving a talk about adaptive reliable hardware in the nano age. This was followed by Peter Cheung’s talk with the topic reconfigurability for variability. The third talk was given by Diana Goehringer, who presented the hardware architecture and the design methodology of a reconfigurable multiprocessor system, called RAMPSoC. After the lunch break Reiner Hartenstein presented the advantages of reconfigurable architectures. The final talk was given by Jim Torresen, who presented a new project at his institute, which focuses on run-time reconfigurable hardware systems.
After each talk, the presenters gave the auditorium some provocative questions based on the global topic: “Future Technologies: Nano Shift or CMOS-based Circuit / Architecture Adaptivity?” After the afternoon coffee break all presenters joined for an interactive panel session on this topic.

Tuesday was devoted to the topic of security, lead by Ingrid Verbauwhede. The first question is, if security is a different or similar application domain as others, such as wireless communication or multimedia. Similar to other application domains, security and cryptographic algorithms need efficient implementations, in terms of throughput, area, power and / or energy. But unique to security applications, is that the implementations themselves need to be secure, e.g. to protect the secret keys or to avoid that sensitive information leaks from the circuit. Protecting sensitive information adds to the area, time and / or energy budget. Hence a trade-off needs to be made. Both topics where covered in the morning and afternoon sessions. Saar Drimer started by proposing methods for fair evaluation of FPGA design and other thoughts on FPGA design security. Patrick Schaumont discussed the topic of PUFs (Physically Uncloneable Functions) or how to enjoy the variability in a FPGA. Dirk Stroobandt discussed the topic of run-time reconfigurable architectures and how it could be used as a security protection mechanism. The topic of IP (Intellectual Property) protection on FPGA is one that received a lot of attention from the audience. First there were two presentations on this topic. Daniel Ziener discussed watermarking and identification techniques for FPGA IP Cores and Nele Mentens presented a research project on secure remote reconfiguration. Mladen Berekovic presented rASIP, a reconfigurable application-specific instruction-set processor. Finally, Jozsef Vasarhelyi gave a talk about Mojette implementations and applications in mobile communication.
In the evening, the panel session continued on this controversial topic. The biggest unsolved problem seems to be the protection of IP (Intellectual Property). In the ideal world, one would like to download an IP core, evaluate it and after evaluation decide to buy it. When you don't buy, you don't have 'access' to the core anymore. How to give a license for a limited use, e.g. for 5 devices? How to make it 'simple' like buying a song from an iTunes store? It was noted that quite some initiatives have already been taken but none have really taken off.

The third day of the seminar (Wednesday) contained just four presentations during the morning (with the presenters invited to be controversial, and a group discussion in the evening).The theme for the day was: “Reconfigurable Architectures in 2020”. The aim was to look far behind today´s architectures and look at possible developments and market margins for reconfigurable technology in about 10 years from now. In a prologue, Jürgen Teich presented the “Bermuda triangle” of reconfigurable computing being spanned by the axis of *flexibility*, *efficiency*, and *productivity*. He suggested future architecture models such as “Sea of FPGAs”, “Co-Pro-Gas” which denote MPSoCs where each core is augmented by an FPGA and heterogeneous MPSoC architectures with FPGAs being used as tile processors. This introduction was followed by four talks of Prof. Yahun Ha from NUS on novel high-speed FPGA interconnection structures including time-multiplexing, Gordon Brebner from Xilinx on their current architecture developments, Oliver Diessel from UNSW on dilation of placement in Dynamic NoC Cores, and finally, Ralf König from KIT on hypermorphic architectures.

On Wednesday afternoon, we had a photo of the participants taken and organized – as is a must when visiting Dagstuhl - a hiking trip – in this case to the Hochwaldalm in Wadrill. The weather luckily was very bright and sunny, and, to several of the participants, unfortunately, too hot. We were chased by German Bremsen that did not leave us alone…. However, last but not least, a bus returned us home safely in the evening just in time before a thunderstorm with flushes of rain came down on

Dagstuhl and we were happy to have a scientific panel discussion moderated by Gordon Brebner on the achievements and unsolved problems in reconfigurable computing. The panelists were Oliver Diessel, Saar Drimer, Andreas Koch and Gerard Smit. Gordon concluded the panel and subsequent discussions with the following statements that technologies and applications are there, but it needs to be put a focus on what high-level tools will be needed to move on from lower-level design methods. Furthermore, design for fault-tolerance could be a main driver of future research as well as the verification of dynamically reconfigurable systems in general which has so far received not enough attention yet.

The gap between reconfigurable architectures and application design environments became the central topic on Thursday with several very interesting contributions. The session began with an introduction by Peter Athanas that emphasized the lacking capabilities of contemporary flows, and that they did not sufficiently cater to dynamically reconfigurable architectures. Lars Bauer gave a presentation titled, “Run-time Adaptation for Reconfigurable Embedded Processors”. Although both DPR and HLS are important future trends regarding hardware design, they develop quite independently. His talk focused on the design and the implementation of a framework combining the two technologies. Lars Braun presented “API to assist the assembly of 2D reconfigurable systems,' where a new concept of using micro blocks for the communication infrastructure as well as for the functional elements on the FPGA was discussed. Robert Hartl presented a deterministic method to determine the AVF (Architectural Vulnerability Factor) of any RT-level circuit using a standard simulation model. Dirk Koch then followed with a new project to address run-time reconfigurable hardware systems. He gave the audience an update on his novel project named Context Switching Reconfigurable Hardware for Communication Systems (COSRECOS), which focuses on architectures for reducing reconfiguration time as well as undertaking tool development. Neil Bergmann proposed a design methodology based on platforms. After this, Gerard Smit presented a mathematical approach towards hardware design. Then, Luigi Carro discussed the role of FPGAs in the near future and presented some challenges for them to reach the general purpose arena. A talk titled “Design and Implementation of an Object-Oriented DPR-Framework” was given by Norbert Abel. The aim of his presentation was to translate common software algorithms to hardware in an efficient way (which is called high-level synthesis or HLS). Although both DPR and HLS are important future trends regarding hardware design, they develop quite independently. Christian Hochberger presented a simulator for AMIDAR (adaptive microinstruction driven architecture) processors.

Finally, on Friday, several talks focusing on the topic: “Applications and More” were given. Reiner Hartenstein gave the first talk of the day with the title “An Approach to Reinvent Programmer Education.” Here, he examined, which productivity user interface should be used for education settings, and, how to provide a sense for locality needed for efficiently programming all possible types of parallelism in heterogeneous systems with many-core and reconfigurable platforms. Afterwards, Sascha Uhrig presented the GAP Processor. This is a Processor with a two-dimensional execution unit. Followed by this, Rene Cumplido outlined a reconfigurable hardware architecture for implementing a LDPC module suitable for software radio systems. Then, Andreas Koch defined for the participants the concept of Geometric Algebra (GA), a generalization of quaternions and complex numbers. This turns out to be a powerful framework for intuitively expressing and manipulating

the complex geometric relationships common to engineering problems. The talk generated quite a bit of discussion. Finally, Walter Stechele presented the research challenges his group has experienced during the last 4 years, when designing a run-time adaptive video-based driver assistance systems.