Modeling and Analysis of Bus Contention for Hardware Accelerators in FPGA SoCs (Artifact)

Francesco Restuccia
TeCIP Institute and Dept. of Excellence in Robotics & AI, Scuola Superiore Sant'Anna, Pisa, Italy
francesco.restuccia@santannapisa.it

Marco Pagani
TeCIP Institute, Scuola Superiore Sant'Anna, Pisa, Italy
Université de Lille, CNRS, Centrale Lille, UMR 9189, CRIStAL, Lille, France
marco.pagani@santannapisa.it

Alessandro Biondi
TeCIP Institute and Dept. of Excellence in Robotics & AI, Scuola Superiore Sant'Anna, Pisa, Italy
alessandro.biondi@santannapisa.it

Mauro Marinoni
TeCIP Institute and Dept. of Excellence in Robotics & AI, Scuola Superiore Sant'Anna, Pisa, Italy
mauro.marinoni@santannapisa.it

Giorgio Buttazzo
TeCIP Institute and Dept. of Excellence in Robotics & AI, Scuola Superiore Sant'Anna, Pisa, Italy
giorgio.buttazzo@santannapisa.it

Abstract

This artifact provides the means for reproducing the experiments presented in the paper "Modeling and Analysis of Bus Contention for Hardware Accelerators in FPGA SoC". In particular, it provides the means and describes how to replicate the experimental study that has been carried out to evaluate the proposed analysis with synthetic workloads.

2012 ACM Subject Classification Hardware → Interconnect; Hardware → Hardware accelerators

Keywords and phrases Heterogeneous computing, Predictable hardware acceleration, FPGA SoCs, Multi-Master architectures

Digital Object Identifier 10.4230/DARTS.6.1.4

Related Article Francesco Restuccia, Marco Pagani, Alessandro Biondi, Mauro Marinoni, and Giorgio Buttazzo, "Modeling and Analysis of Bus Contention for Hardware Accelerators in FPGA SoCs", in 32nd Euromicro Conference on Real-Time Systems (ECRTS 2020), LIPIcs, Vol. 165, pp. 12:1–12:23, 2020. https://doi.org/10.4230/LIPIcs.ECRTS.2020.12

Related Conference 32nd Euromicro Conference on Real-Time Systems (ECRTS 2020), July 7–10, 2020, Virtual Conference

1 Scope

The code included in this artifact models an AXI system consisting of a set of hardware accelerators (HW-tasks) connected to a shared system memory through a set of AXI interconnects organized in a hierarchical manner. The main objective of the proposed model is to evaluate the impact of the AXI topology on the system schedulability utilizing the real-time analysis presented in Section 4. In particular, this artifact allows replicating the experiments presented in Section 5.4, showing how the schedulability ratio for an AXI system varies while varying the system topology and the workload generated by the HW-tasks.

2 Content

The root directory of the artifact package archive contains the documentation for setting up the system and replicating the experiments. The documentation is available both in Markdown and HTML:

- `readme_ecrts_2020_ae.html`
- `readme_ecrts_2020_ae.md`

Then, the `sim` sub-directory contains the actual code of the AXI model:

- `axi_system.py`: models an AXI system consisting of a set of HW-tasks connected through a set of AXI interconnects to a shared memory;
- `axi_topology.py`: models the topology of an AXI system (i.e., the arrangement of HW-tasks ad interconnects);
- `axi_workload.py`: models the workload generated by the HW-tasks;
- `taskgen.py`: contains an implementation of the *fixedrandsum* algorithm used for generating the workload;
- `experiments.py`: contains the code for generating the AXI system used in the experiments and replicating the evaluation.

3 Getting the artifact

The artifact endorsed by the Artifact Evaluation Committee is available free of charge on the Dagstuhl Research Online Publication Server (DROPS).

4 Tested platforms

The AXI system model has been implemented with Python version 3. The code has been run and tested on a multicore desktop computer running Fedora Workstation 30 x86_64. Being coded in Python, the artifact is platform-independent and not assume or require any particular hardware configuration. Hence, it should work on any system providing the following packages:

- `Pyhton 3.x`;
- `NumPy`;
- `Matplotlib`;
- `NetworkX`.

The instruction included in the artifact describes how to replicate the experiments on a typical GNU/Linux environment using Ubuntu and derived distributions or Fedora Workstation and derived distributions. Please consider that running artifact experiments may take a substantial amount of time. For instance, an entire run may take up to 12 hours on a standard desktop multicore PC. However, the code has been designed to take advantage of modern multicore platforms. Hence, please consider using a dedicated machine having eight or more processing cores for replicating the experiments in a reasonable amount of time.

5 License

6 MD5 sum of the artifact

0228fd08ccc8ebd51b3e6cb1eabdb486

7 Size of the artifact

12 KiB