

# **14th Workshop on Parallel Programming and Run-Time Management Techniques for Many-Core Architectures**

# **12th Workshop on Design Tools and Architectures for Multicore Embedded Computing Platforms**

PARMA-DITAM 2023, January 17, 2023, Toulouse, France

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## ■ Preface

This volume collects the proceedings of the PARMA-DITAM workshop 2023. PARMA-DITAM brings together the decade-long experience of two workshops: the workshop on Parallel Programming and Run-Time Management Techniques for Many-core Architectures (PARMA) and the workshop on Design Tools and Architectures for Multicore Embedded Computing Platforms (DITAM). These events first joined in 2014 and since then they represented a reference point in the European community of high-performance computer architectures, embedded systems and compiler technologies. PARMA-DITAM is co-located with and sponsored by the HiPEAC conference, which annually gathers the most excellent researchers on High Performance Embedded Architectures and Compilers within the European borders and beyond.

The PARMA-DITAM 2023 workshop includes topics such as parallel programming models, design space exploration tools and run-time management techniques aiming at exploring the features and performance of different computing architectures, possibly heterogeneous, (re-)programmable and/or (re-)configurable, spanning from embedded and cyber-physical systems, to high performance computing platforms.

This edition features 4 regular papers, carefully selected among 6 submissions by our expert Technical Program Committee after a double-blind review process. The editors are proud to propose, in the early pages of this volume, 3 additional manuscripts from invited research groups, who presented their research and results in invited talks during the workshop event.

The PARMA-DITAM workshop focuses on seven main topics:

- Parallel programming models and languages, compilers and virtualization techniques
- Runtime modelling, monitoring, adaptivity, and management
- Runtime trade-off execution, power management, and memory management
- Heterogeneous and reconfigurable many-core: architectures and design space exploration
- Methodologies, design tools, and high level synthesis for many-core architectures
- Parallel applications for many-core platforms
- Case studies, success stories and applications applying T1–T6

The editors invites researchers to submit their future works for consideration in the subsequent editions of this workshop.

João Bispo, Henri-Pierre Charles, Stefano Cherubin, and Giuseppe Massari



